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№ 3125

Modelling & Simulation of 19-level Cascaded Hybrid Multilevel Inverter with less number of Switches

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April 7, 2020

MODELLING & SIMULATION OF 19-LEVEL CASCADED HYBRID MULTILEVEL INVERTER WITH LESS NUMBER OF SWITCHES

MANUSCRIPT TRACK: ADVANCED POWER SYSTEMS,

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Abstract:
In 21st century, we can't imagine a single day without electrical appliances and the most important thing is to get uninterrupted power supply. Inverter is the essential part to design an uninterrupted power supply system. This paper presents the modelling and simulation of 19-level cascaded hybrid multilevel inverter (MLI) having less number of switches. MLI is one of the most efficient power converters which are especially suited for high power applications with reduced harmonics. MLI not only achieves high output power but also used in renewable energy sources such as photovoltaic, wind and fuel cells. The main objective of this paper is to get alternating quantity by using cascaded MLI with unequal DC sources called asymmetric cascaded MLI which requires reduced number of power switches. The proposed technology is based on the concept of the ratio of weights in weight box as 5:2:2:1. As it provides a multi stage alternating output based on predefined frequency, so this proposed one can be used for UPS, HVDC transmission system for getting higher efficiency.

Keywords:
MLI, Inverter, HVDC Transmission, Asymmetric cascade inverter.

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I. INTRODUCTION

The inverters are relied upon to provide sinusoidal yields yet the most of the available inverters produce non-sinusoidal output and subsequently contain a high level of harmonics distortion. So to design a close sinusoidal component with the reduced harmonic distortion, multilevel inverters are the best suitable option. This proposed methodology can be used for electric vehicle, HVDC power transmission and UPS design mostly. Among the different multilevel structures that were introduced by researchers, the cascaded multilevel inverter[4][5] turns out to be much predominant in harmonic reduction. Further, the harmonics of lower order which are present in the output of any inverter can be minimized by changing different switching strategies and asymmetric sources. To eliminate the lower order harmonics, the technology that was developed, named as Selective Harmonic Elimination Pulse Width Modulation (SHEPWM)[5] technique for multilevel inverters. The trigonometric terms in the equations provide multiple solutions thereby, making it complex to control the switching angle and hence reduce the lower order harmonics[4]. To suppress the lower order harmonics, the control of the switching angles of inverters is very important and that can be achieved by that arithmetic solution. Several researches were carried out to solve these equations by mathematical methods and evolutionary algorithms. And the mathematical methods are based on derivative process and needs some initial assumptions. Different topologies[3] were developed like capacitor-clamped, diode-clamped inverter and cascaded multilevel inverter with separate values of DC sources. An optimal switching technique was proposed to reduce the switching losses, but due to high output currents and series connection of several semiconductors this technique had more conduction losses. Despite the fact that different novel algorithms for Selective Harmonic Elimination were created, yet they slacked in the capacity to take out substantial number of low order harmonics. This lead to the advancements in selective harmonic elimination pulse width modulated technique based on the foraging behaviour of a colony of ants.

In recent years multilevel inverter plays an important role and attracts more attention in the conversion of medium power applications. It is simple in construction, better-quality in performance and produces lesser harmonics and having lower switching losses, with reduced switching stresses[3] and harmonics. The three

commercial topologies of multilevel voltage source inverters are (i) the Neutral Point Clamped (NPC) or diode clamped multilevel inverter (DCMLI), (ii) flying capacitor multilevel inverter (FCMLI) and (iii) cascaded H bridge (CHB) multilevel inverter[2][5]. Unlike DCMLI and FCMLI the CMLI does not require voltage clamping diodes and voltage balancing capacitors. This paper focuses particularly on cascaded hybrid multilevel inverter which requires several no of independent DC sources with different values. Multilevel strategies which are available till now, if we use "n" number of DC sources the number of levels can be obtained is $(2n + 1)$[1]. And based on the DC source used, the CHB multilevel inverter is further divided into two topologies namely symmetric and asymmetric inverters. The values of all the voltage sources are equal in symmetric topology[1][3]. In symmetric topology if we want to increase the number of output voltage levels, we have to increase in number of switching devices. So in order to achieve the more number of output voltage levels with less number of switching devices, we have to use the different value of DC sources, which is named as asymmetric topology. Among these two topologies, asymmetric cascaded MLI is explained in this paper and it requires four no of unequal DC sources to produce nineteen-level output. This new topology has been proposed to obtain 19-level output with minimum number of switches. In addition to that the THD are reduced and some specified lower order harmonics[6] are also eliminated by using selective cascaded harmonic elimination pulse width modulation (SCHE PWM) technique.

II. METHODOLOGY

The proposed system takes a user defined input frequency to calculate the switching time by considering a particular levelled output. And basis on the switching time, switching pulse is being generated and feeded to the selecting switches to generate a levelled output and based on the condition of bridge switches, the alternating voltages is experienced by the load. A normal H bridge inverter and some auxiliary switches with some un-identical sources are used for this proposed system. A stepped waveform is generated at the output according to how the sources are being connected to the load. The H Bridge is used normally to produce alternating voltage output. To reduce the internal circuitry and overheating of the circuit, different level of voltages is being used which tends to reduce the number of switches. Here we have considered the output voltage level at '(+ve)9' to '(-ve)9 volt as a reference and to reduce the number of switches the value of sources have been considered at a ratio of 5:2:2:1. In this particular format we can easily get the different voltage level by connecting the different sources

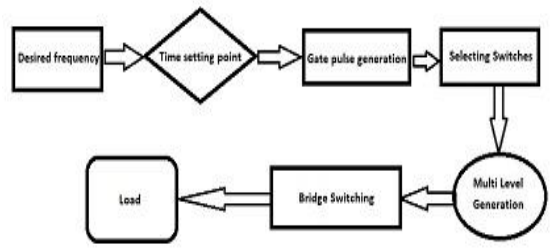

Fig.1: Block diagram of proposed model

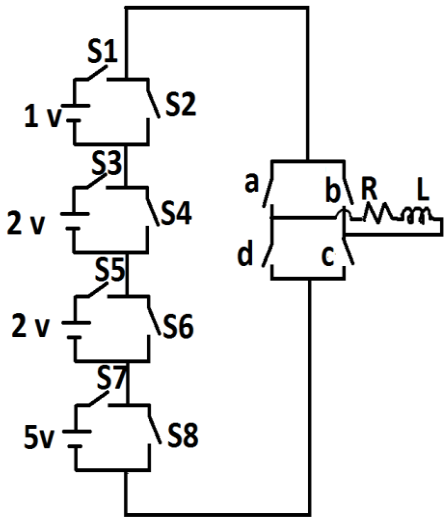

Fig.2: Circuit model

simultaneously just like the weigh box concept. During the positive half cycle, switches 'a' and 'c' are always turned on and the level selecting switches are operated to get different voltage levels as per our choice. To generate the negative half cycle, switches 'b' and 'd' are conducting while the level selecting switches are operated to get a staircase voltage at the output. To obtain the first level, the dc source of V_1(1v) must be connected to the load. To generate the second level, V_2(2v) must be connected to the load and to obtain the third level both V_1 and V_2 must be connected and will continues till the last level. The switches are controlled in such a way that respective sources are connected to the load during desired time intervals.

III. EXPERIMENTATION

The new design of multilevel inverter is required to reduce the number of switches to form an asymmetric inverter. The circuit diagram of 19 level multilevel inverter is shown in fig 3.

Here there are 4 numbers of dc sources which are connected with IGBT switches which makes an h-bridge inverter. This is the main circuitry of our proposed 19 level multilevel inverter. All IGBT switches are connected as shown in fig.2 in order to form a hybrid cascade inverter. The gate signal for 19 level inverter is generated for triggering the 8 main IGBT (selecting switch) to get the optimum output. The main purpose of the other four IGBT (bridge switch) is to control the output for the positive and negative half. For first positive half cycle switch 'a' & 'c' will be close & switch 'b' & 'd' will be open and for the very next negative half cycle switch 'b' & 'd' will be close & switch 'a' & 'c' will be open.

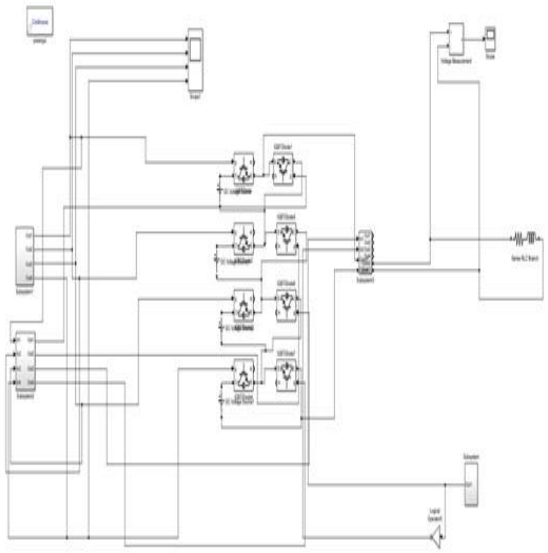

Fig.3: Experimental circuit model

The switching sequence will be as follows:

For positive half cycle bridge switch 'a'& 'c' are always in **ON stage** and switch 'b'& 'd' are always in **OFF stage**

1. When S2,S4,S6,&S8 are **ON** then output voltage is 0v
2. When S1,S4,S6,&S8 are **ON** then output voltage is 1v
3. When S2,S3,S6,&S8 are **ON** then output voltage is 2v
4. When S1,S3,S6,&S8 are **ON** then output voltage is 3v
5. When S2,S3,S5,&S8 are **ON** then output voltage is 4v
6. When S2,S4,S6,&S7 are **ON** then output voltage is 5v
7. When S1,S4,S6,&S7 are **ON** then output voltage is 6v
8. When S2,S3,S6,&S7 are **ON** then output voltage is 7v
9. When S1,S3,S6,&S7 are **ON** then output voltage is 8v
10. When S2,S3,S5,&S7 are **ON** then output voltage is 9v
11. When S1,S3,S6,&S7 are **ON** then output voltage is 8v
12. When S2,S3,S6,&S7 are **ON** then output voltage is 7v
13. When S1,S4,S6,&S7 are **ON** then output voltage is 6v
14. When S2,S4,S6,&S7 are **ON** then output voltage is 5v
15. When S2,S3,S5,&S8 are **ON** then output voltage is 4v
16. When S1,S3,S6,&S8 are **ON** then output voltage is 3v
17. When S2,S3,S6,&S8 are **ON** then output voltage is 2v
18. When S1,S4,S6,&S8 are **ON** then output voltage is 1v
19. When S2S4,S6,&S8 are **ON** then output voltage is 0v

For negative half cycle bridge switch 'b'& 'd' are always in **ON stage** and switch 'a'& 'c' are always in **OFF stage** and the selecter switching sequence will remain same.

Table.1: Switch condition

Selecting switches (ON)	**Selecting switches (OFF)**	**Bridge switches (ON)**	**Bridge switches (OFF)**	**Output level in voltage**
S1,S4,S6,S8	S2,S3,S5,S7	A,C	B,D	1V
S2,S3,S6,S8	S1,S4,S5,S7	A,C	B,D	2V
S1,S3,S6,S8	S2,S4,S5,S7	A,C	B,D	3V
S2,S3,S5,S8	S1,S4,S5,S7	A,C	B,D	4V
S2,S4,S6,S7	S1,S3,S5,S8	A,C	B,D	5V
S1,S4,S6,S7	S2,S3,S5,S8	A,C	B,D	6V
S2,S3,S6,S7	S1,S4,S5,S8	A,C	B,D	7V
S1,S3,S6,S7	S2,S4,S5,S8	A,C	B,D	8V
S2,S3,S5,S7	S1,S4,S6,S8	A,C	B,D	9V
S2,S4,S6,S8	S1,S3,S5,S7	A,C	B,D	0V

S1,S4,S6,S8	S2,S3,S5,S7	B,D	A,C	-1V
S2,S3,S6,S8	S1,S4,S5,S7	B,D	A,C	-2V
S1,S3,S6,S8	S2,S4,S5,S7	B,D	A,C	-3V
S2,S3,S5,S8	S1,S4,S5,S7	B,D	A,C	-4V
S2,S4,S6,S7	S1,S3,S5,S8	B,D	A,C	-5V
S1,S4,S6,S7	S2,S3,S5,S8	B,D	A,C	-6V
S2,S3,S6,S7	S1,S4,S5,S8	B,D	A,C	-7V
S1,S3,S6,S7	S2,S4,S5,S8	B,D	A,C	-8V
S2,S3,S5,S7	S1,S4,S6,S8	B,D	A,C	-9V

IV. RESULTS AND DISCUSSION

Here is the different switching signal, which is being generated by the time setting block used in MATLAB and feeded to the IGBTs and based on that switching signal, we have achieved our target levelled output.

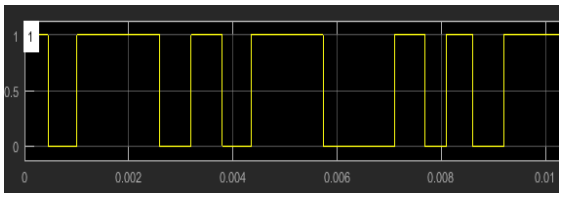

Fig.4: Switching signal 1

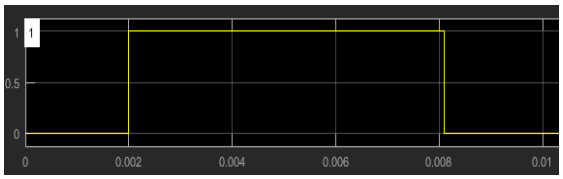

Fig.5: Switching signal 2

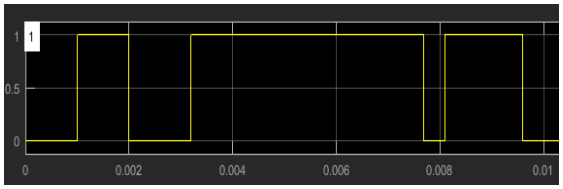

Fig.6: Switching signal 3

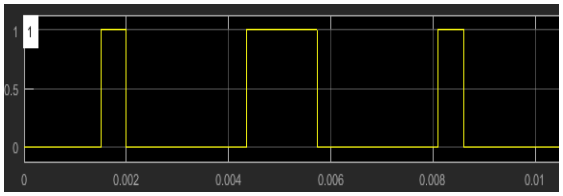

Fig.7: Switching signal 4

After successful operation of all the switches, the expected result looks like the below mentioned figure 8.

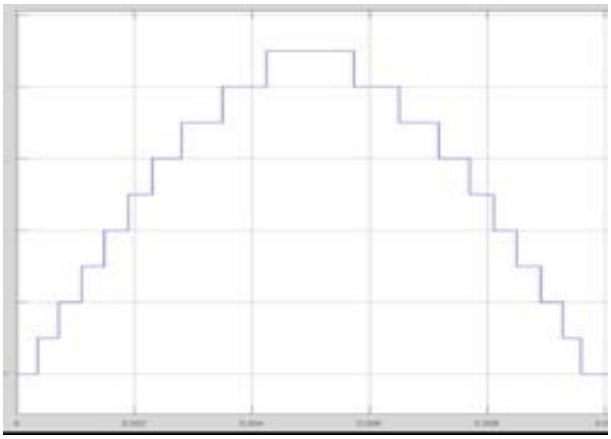

Fig.8: Output for +ve half cycle

The output result is not a pure sinusoidal wave, but closes to the sinusoidal form of positive half cycle and the similar steps in negative region for the other half cycle also. The harmonic distortion is also minimised compare to other lower level inverter system. For a seven level cascaded multilevel inverter[1] THD at simulation level was at 11.51% whereas our proposed system shows only 8.47% of THD.

V. CONCLUSIONS

The proposed system is capable to deal with high voltage and high power cascaded hybrid multilevel inverter with uneven DC voltage sources. And the complete simulation model of a cascaded multilevel inverter system has been proposed by using MATLAB/Simulink programming. As the system clearly shows the output closer to the sinusoidal form with a reduced harmonic distortion, so we can use the system to design an uninterrupted power supply, inverter system as well as in the converter station for a HVDC transmission system.

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