EasyChair Preprint

№ 4794

DSP-based Digital Control Techniques for Interleaved Boost PFC Converter

Phu Hieu Pham, Anh Dung Nguyen and Huang-Jen Chiu

December 25, 2020

DSP-based Digital Control Techniques for Interleaved Boost PFC Converter

Phu Hieu Pham, Anh Dung Nguyen
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, Virginia, U.S.A
Email: pphieu@vt.edu

Huang-Jen Chiu
Department of Electronics and Computer Engineering
National Taiwan University of Science and Technology
Taipei, Taiwan (R.O.C)

***Abstract*—This paper introduces an interleaved boost power factor correction (PFC) converter using digital controller. Current sample correction (SC), duty ratio feedforward (DFF) and adaptive PID compensator methods are employed to improve the overall circuit performance. A 3-kW prototype has been built to verify the feasibility of proposed digital controller**

Keywords—interleaved boost PFC, sample correction, duty ratio feedforward, adaptive PID compensator

I. INTRODUCTION

Nowadays, an interleaved boost converter is widely used in high power, high voltage AC-DC [1]. The PFC circuit always employ two control loops: the inner loop called current loop, which has to shape the current waveform, and the outer loop called voltage loop, which control the output DC voltage by providing the reference signal for the current loop. Current loop must have very high bandwidth since it has to control the input current to follow a sinusoidal trajectory. The bandwidth of voltage loop is much lower than that of the current loop since the output voltage is expected to stay at a fixed reference voltage and insensitive to control noise. For high power application, boost PFC is usually designed to work in interleaved mode as showed in Fig. 1. Moreover, continuous conduction mode (CCM) operation is preferred as compared with discontinuous conduction mode (DCM) to reduce the current stress on devices and hence, averaged current mode control is applied for this kind of converter due to high power factor (PF) and low total harmonic distortion (THD). There are also a lot of commercial analog controller that support Boost PFC working in this mode such as UC3854[2] or NCP1563[3]. In the past, analog PFC controller are more preferable over digital PFC controller since they are more cost-effective. However, this is changing nowadays since digital controller are becoming cheaper and it has so many advantages over its analog counterpart, such as lower component count, the degree of complexity depends upon the algorithm, and the flexibility of implementing different control methods that make it become more appeal to industry.

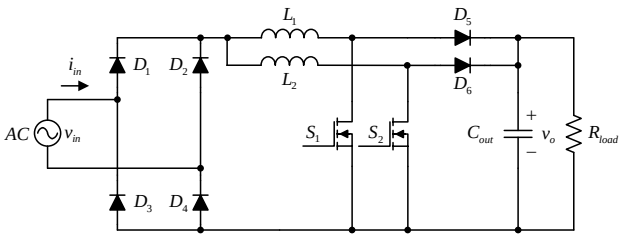

Fig. 1. Two phases interleaved Boost PFC converter

In this paper, current sample correction, duty ratio feedforward and adaptive PID compensator techniques implemented by digital controller are presented to improve the performance of circuit. A 3-kW interleaved boost PFC prototype using integrated digital controller UCD3138 of Texas Instruments has been built to verify the feasibility of proposed digital control techniques. The experimental results showed that PF is greater than 0.92, and THD is lower than 7% in all cases.

II. THE PROPOSED DIGITAL CONTROL METHODS

A. Current Sample Correction

In boost converter, there are two conduction modes: continuous conduction mode (CCM) in Fig. 2(a) and discontinuous conduction mode (DCM) in Fig. 2(b). The state at the transition between DCM and CCM is called boundary mode operation. When the converter works in boundary mode operation, the average input current is:

$$\langle i_L \rangle = \frac{dTv_{in}}{2L} \tag{1}$$

Lower value of average input current will result in DCM operation. On the other hand, higher value will result in CCM operation. In order to control the trajectory of current waveform using digital controller, the average current in one switching cycle need to be measured. The simplest way to measure the average current is sampling at the instance of current in the middle of the rising edge of the inductor current [4]. During CCM, the average input current $<i_L(nT)>$ equals the input current sample $i_L(nT)$. However, in DCM, the actual average input current is smaller than the input current sample [5].

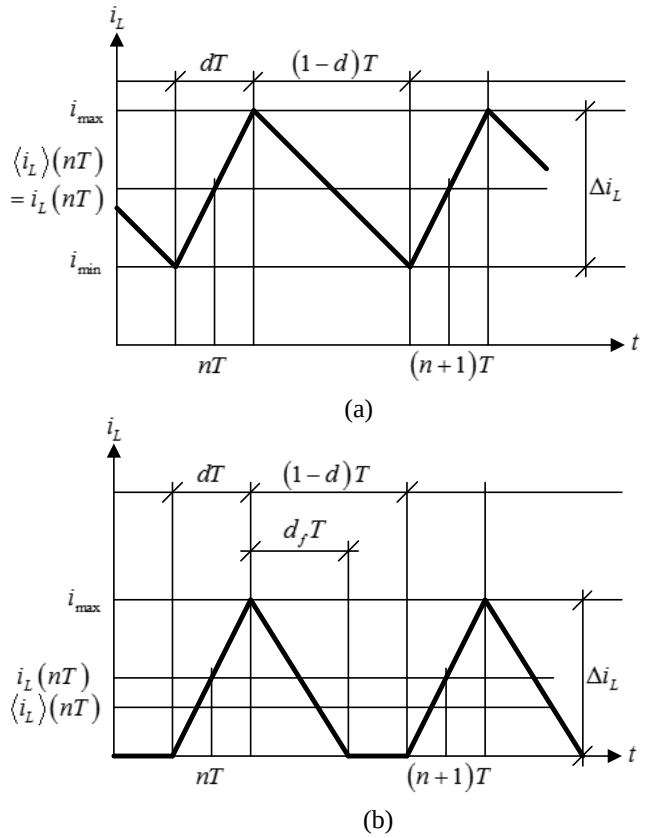

Fig. 2. Inductor current waveform in (a) CCM and (b) DCM

Since the input current is sampled at the middle of the rising edge, the relationship between input current sample and maximum current is given by:

$$i_L(nT) = \frac{i_{max}(nT)}{2} \tag{2}$$

Referring to Fig. 2, the average input current within one switching cycle can be calculated by:

$$\langle i_L \rangle (nT) = \frac{i_{max}(nT)}{2} \frac{(d+d_f)T}{T} = (d+d_f)\frac{i_{max}(nT)}{2} \tag{3}$$

Substitute (2) into (3) yields:

$$\langle i_L \rangle (nT) = (d+d_f) i_L(nT) \; @ \kappa(nT) i_L(nT) \tag{4}$$

where $k(nT) = d+d_f$ represents the fraction within one switching period where $i_L \neq 0$. In CCM, $k = d+d_f = 1$, the input current i_L never returns to zero. In DCM, $k<1$, this makes the average input current always smaller than the input current sample. Consequently, Eq. (4) is correct for both DCM and CCM. When programming the compensators, d is the output of the current compensator, but d_f is unknown. Hence, it it necessary to derive a formula for $k(nT)$ without d_f. By applying Volt-Second balance during dT and d_fT, we have:

$$dTv_{in} = d_f T (v_{out} - v_{in}) \tag{5}$$

Hence,

$$d_f = d \frac{v_{in}}{v_{out} - v_{in}} \tag{6}$$

$$\kappa(nT) = d + d_f = d + d \frac{v_{in}}{v_{out} - v_{in}} = \frac{dv_{out}(nT)}{v_{out}(nT) - v_{in}(nT)} \tag{7}$$

Equation (7) is used to calculate the correction factor in DCM. However, as mentioned earlier, in CCM, by definition, this correction factor equals 1. Therefore, (7) can be used for both DCM and CCM operations, and the detection for DCM and CCM is not necessary, which is an advantage of the algorithm. Fig. 3 depicts the block diagram of the algorithm.

B. Duty Ratio Feedforward

When the averaged current mode control is applied, the input current of boost PFC converter leads the input voltage [6], resulting in a non-unity fundamental displacement power factor and the zero-crossing distortion. Since interleaved topology is a combination of two single Boost circuit, this effect still remains. The reason is that the average switch voltage v_s delayed over a time LG_e (G_e is the desired input admittance of the boost PFC converter) compared with the input voltage v_{in} [7], as shown in Fig. 4. This implies that a feedforwarded duty-ratio d_{ff}^{ccm}, which resulting in the average switch voltage equals to the input voltage, can be added to the output of the current compensator. By doing this, instead of having to reconstruct the entire v_s, the task of current compensator reduces to compensating the small different between v_{in} and v_s. Consequently, the resulting inductor current tracks its reference value more easily. When a boost converter works in CCM, the relationship between the output voltage and the average switch voltage is:

$$v_s = (1-d) v_o \tag{8}$$

The feedforwarded switch voltage resulting from the feedforward duty-ratio d_{ff} is:

$$v_{s,ff} = v_{in} \tag{9}$$

The value for d_{ff}^{ccm} can be calculated as following:

$$d_{ff}^{ccm} = 1 - \frac{v_{s,ff}}{v_o} \; ; \; 1 - \frac{v_{in}}{v_o} \tag{10}$$

Whereas, in DCM, duty feedforward is expressed as following equation:

$$d_{ff}^{dcm} = \sqrt{2 \frac{L}{T} \frac{\langle I_L \rangle}{V_{in}} \frac{V_o - V_{in}}{V_o}} = \sqrt{\frac{2G_e L}{T} d_{ff}^{ccm}} \tag{11}$$

In most of cases of the operating conditions, within half of grid cycle, the inductor current appears to be in both DCM and CCM operations, with DCM operation happens near the zero-crossing of the input voltage. Hence, the duty ratio feedforward for mixed conduction mode (MCM) is derived:

$$d_{ff}^{mcm} = \min\left(d_{ff}^{dcm}, d_{cc}^{ccm}\right) \tag{12}$$

The overall algorithm that combines current sample correction and duty ratio feedforward is depicted on Fig. 5.

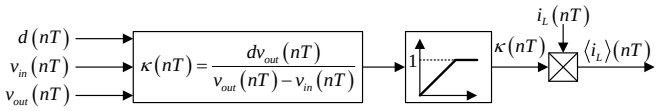

Fig. 3. Current Sample Correction algorithm

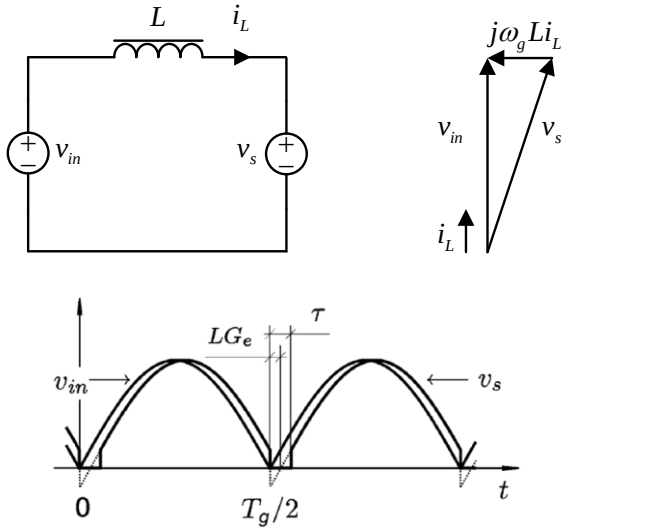

Fig. 4. Simplified model of power stage of PFC converter and the relationship between input voltage and average switch voltage

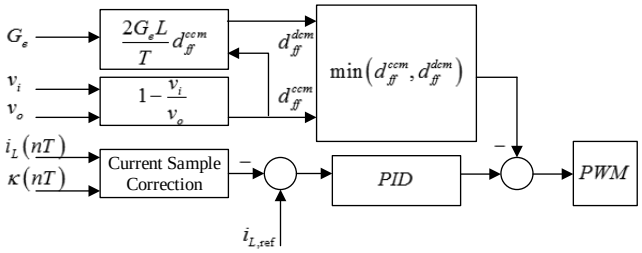

Fig. 5. Current control scheme with Current Sample Correction and Duty Ratio Feedforward for MCM

C. *Adaptive PID compensator*

This method is used independent of sample correction algorithm and duty ratio feedforward methods. As we know, the duty-ratio to output-current transfer functions for DCM and CCM operations are different. Consequently, the dynamics of the current loop change abruptly within one half of the grid cycle when the inductor current changes from CCM to DCM. This is one of the reason which worsen the current waveform near zero-crossing points of input voltage. Secondly, observations from experiments show that, the derivative portion of the current compensator does not have much impact on the current waveform near zero-crossing-points of input voltage. And thirdly, most important of all, the integral portion of the current compensator seems to worsen the current waveform near zero-crossing points of input voltage. Setting the integral coefficient to zero greatly improve the current waveform near zero-crossing points. These analyses lead to a method to improve the current waveform in order to reduce THD, that is using different coefficient sets for different range of instantaneous input voltage:

- Region 1: $v_{in}(t)$ < 50V. DCM operation is inside this region. The integral and derivative coefficients, k_i and k_d, are set to zero. Only $k_p \neq 0$.
- Region 2: $v_{in}(t)$ > 100V. The coefficients set for this region is chosen normally.
- Region 3: Between region 1 and region 2. The coefficients set for this region is the average of coefficients for region 1 and region 2.

III. Experimental Verification

To verify the above methods, a 3-kW 2-phase interleaved boost PFC converter prototype has been built. The input voltage for testing are at 115Vac and 230Vac. Output voltage is 390Vdc with 10V voltage ripple. Two 260µH boost inductors for interleaved topology are calculated and used to match 10% THD requirement. Fig. 6 and Fig. 7 show the experimental waveforms using SC and DFF at 115Vac input – 100% load and 230Vac input – 10% load, respectively. It could be seen that the input current still non-sinusoidal partly. In Fig. 8 and Fig. 9, when employing Adaptive PID compensator, the input current waveform is nearly sinusoidal even in high-line light-load condition. Table I shows the PF and THD comparison of 3 control methods: conventional PID compensator, SC and DFF, Adaptive PID compensator. Theoretically, SC and DFF methods should achieve good results as Adaptive PID compensator. However, it is clearly to see that PF and THD achievement of SC and DFF method still be worse than Adaptive PID compensator. The reason of these results is that the design and implementation of inductor current sense circuit is not good and the current feedback does not reflect exactly the real inductor current.

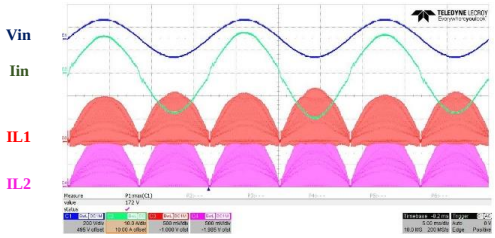

Fig. 6. Measured waveforms using SC and DFF at 115Vac input – 100% load

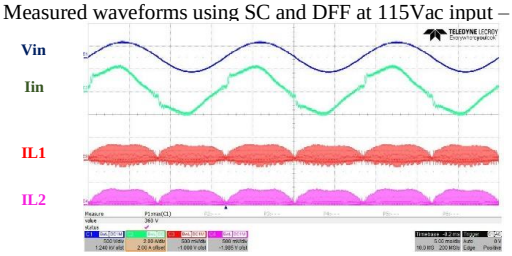

Fig. 7. Measured waveforms using SC and DFF at 230Vac input – 10% load

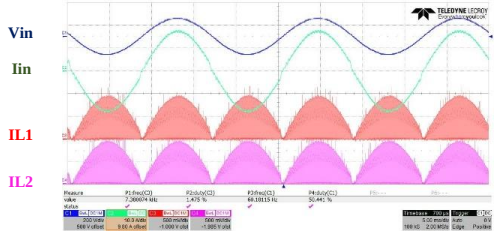

Fig. 8. Measured waveforms using adaptive PID compensator at 115Vac input -100% load

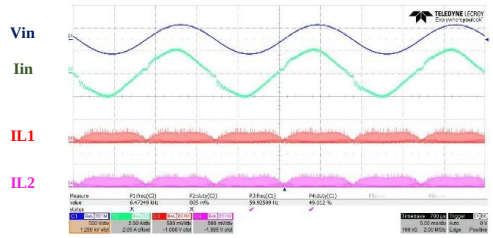

Fig. 9. Measured waveforms using adaptive PID compensator at 230Vac input – 10% load

TABLE I. PF and THD comparison

V_{in}	Load	PF			THD (%)		
		Fixed PID	SC& DFF	Adaptive PID	Fixed PID	SC& DFF	Adaptive PID
115 V	10%	0.97	0.98	0.98	17	11.5	7
	100%	0.99	0.99	0.99	3	2.9	2.9
230 V	10%	0.92	0.93	0.94	10.5	9.2	7.1
	100%	0.99	0.99	0.99	4	4	4

IV. CONCLUSION

The digital control techniques are proposed for 2-phase interleaved boost PFC converter. A 3-kW prototype has been built and tested to verify the feasibility of proposed control methods. Experimental results showed that the THD is reduced to less than 10% with using sample correction and duty ratio feedforward. The results are not good as of using adaptive PID compensator (less than 7% in all cases) but SC and DFF are promising methods and regular for commercial products.

REFERENCE

[1] K. Mahmud and T. Lei, "Power factor correction by PFC Boost topology using average current control method", Proc. IEEE Global High Tech Congr. Electron., pp. 16-20, 2013.

[2] Bill Andreycak, “Optimizing Performance in UC3854 Power Factor Correction Applications”, Design Node DN-39E, Texas Instruments, 1999.

[3] Joel Turchi, “Four Key Steps to Design a Continuous Conduction Mode PFC Stage Using the NCP1653”, Application Note AND8184/D, On Semiconductor, 2004.

[4] D. M. Van de Sype , K. De Gusseme , A. P. Van den Bossche and J. A. A. Melkebeek, "A sampling algorithm for digitally controlled Boost PFC converter", IEEE Trans. Power Electron., vol. 19, no. 3, pp. 649-657, 2004.

[5] K. De Gusseme, D. M. Van de Sype, A. P. Van den Bossche, and J. A. Melkebeek, “Digitally controlled Boost power factor correction converters operating in both continuous and discontinuous conduction mode,” IEEE Trans. Ind. Electron., vol. 52, pp. 88-97, Fe. 2005.

[6] J. B. Williams, "Design of feedback loop in unity power factor AC to DC converter," on PESC '89 record, 20th Annual IEEE Power Electronics specialists conference, vol. 2, pp. 959-967, Jun. 1989.

[7] David M. Van de Sype, K. De Gusseme, A. P. M. Van den Bossche, and J. A. Melkebeek, "Duty-ratio feedforward for digitally controlled Boost PFC converters," IEEE trans. Industrial Electron., vol. 52, no. 1, pp. 108-115, Feb. 2005.