



## On Test Circuit Design on Predicate Integrated Circuit with Logic Simulation Tool

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Frank Appiah

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# ON TEST CIRCUIT DESIGN ON PREDICATE INTEGRATED CIRCUITS WITH LOGIC SIMULATION TOOL.

Frank Appiah, Professional

**Abstract**—This article is on test circuits designed to check a functional logic based on the digital circuits embedded in the integrated circuits developed from [11]. The testing of integrated circuits are described in this article with schematic capture of circuits. A complete setup of switching components are made in the process of defining the connection switches. Finally, this research demonstrates an example of IC testing outputs with computer-aided design(cad).

**Index Terms**—digital circuit, logic circuit, design, simulation, integrated circuit, truth table, tool, cad, timing diagrams.

• Frank Appiah is with King’s College London, King’s Engineer Group, UK. E-mail: [appiahnsiahfrank@gmail.com](mailto:appiahnsiahfrank@gmail.com)

## 1 INTRODUCTION

With variables MbA and MbNg,

These logic functions are generated[11]:

(1)	$\overline{MbA} \cdot MbNg + MbA \cdot \overline{MbNg}$
(2)	$MbA \cdot \overline{MbNg} + \overline{MbA} \cdot MbNg$

In setting up an IC for MbANbW logic gate circuit, Logic Circuit Sim Professional (full version) was used in achieving this. With single selection mode activation, the following are labelled IO points in orange color in the preview after :

- 1.MbA
- 2.MbNg
- 3.IO\_or
- 4.IO\_Xor.

The next setup for MbAMbNg logic circuit is shown in the steps below in the schematic captures in [11].

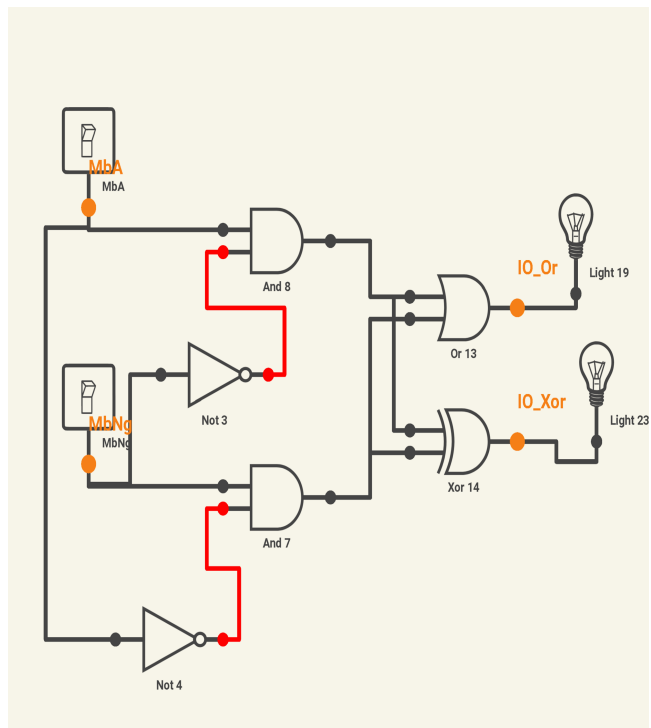


Figure 1.

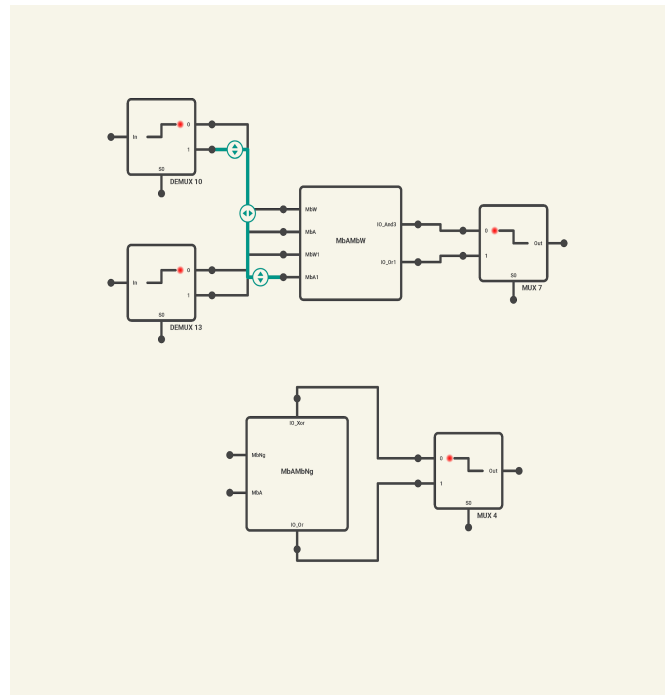
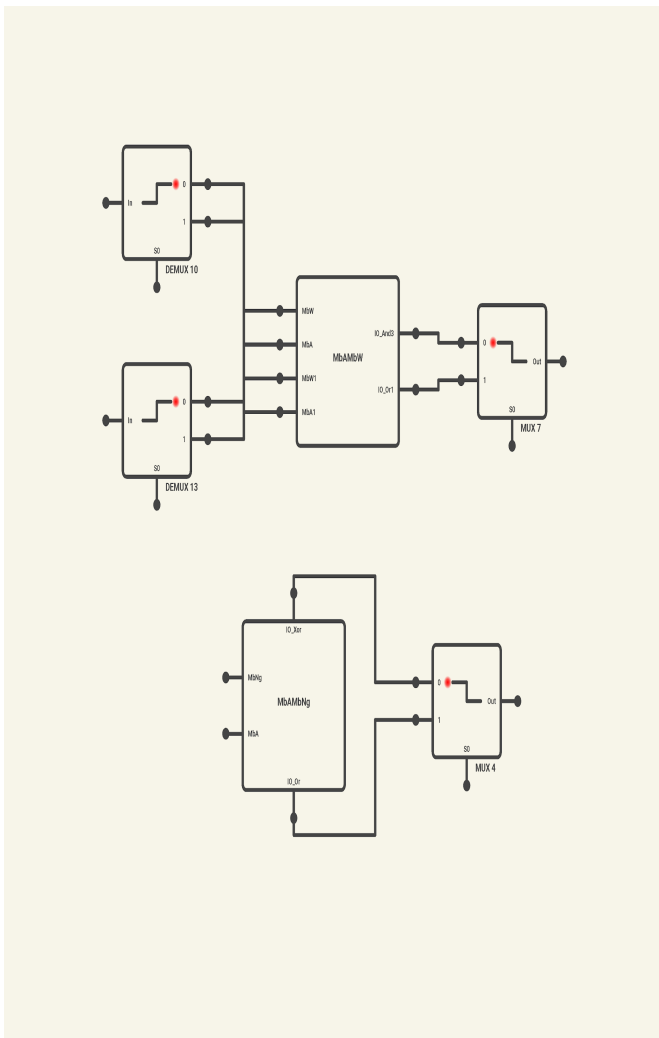
The next stage is to show the completed ic elements in use. I started a new project then add the elements from the ic menu. The menu shows the ic elements of MbAMbW and MbAMbNg logic circuits.[11]

To use is by just selecting them and these appears in the grid layout. These are as shown below in the schematic} : Figure 2.

There are two inputs and two outputs for each embedded circuit/integrated circuit. A demultiplexer is placed in connection to each input to enable selection of one input at a time. For example, MbA and MbA1 inputs to select which is which, a select signal s will enable MbA if s=0 and enable MbA1 if s=1.

The circuit indication for that as described is shown below in the schematic capture :

Figure 3.



The rest of selection for input connections are shown also below in the schematic captures :

Figure 4.

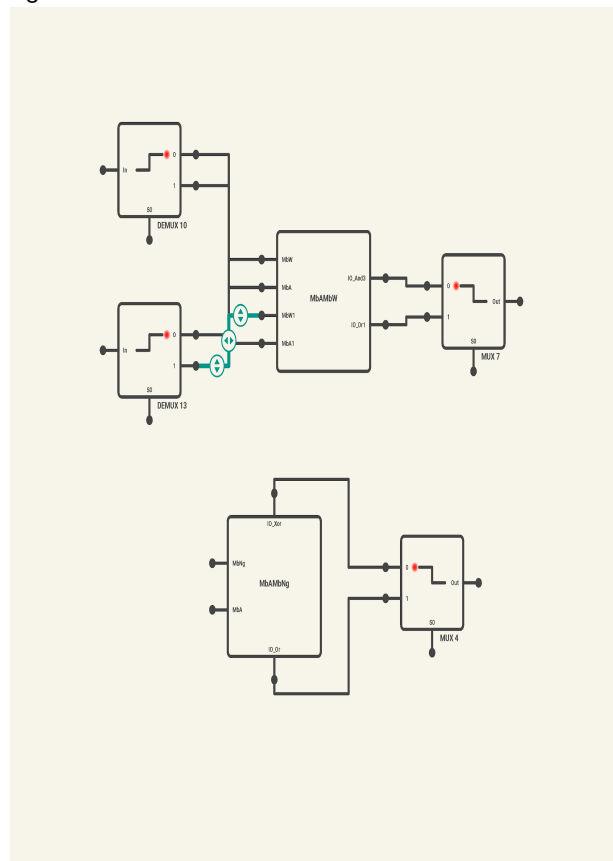


Figure 5.

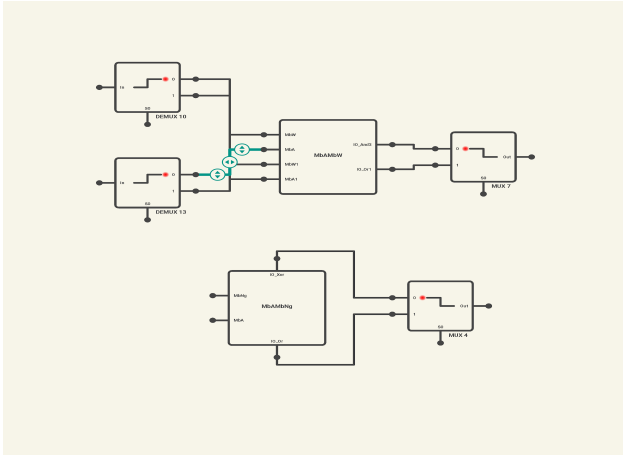


Figure 6.

On the output connection is also a multiplexer to select one output at a time. For MbAMbW ic, the outputs are IO\_And3 which is selected when s=0 and IO\_or1 when s=1 from MUX 7 multiplexer. For MbAMbNg ic, the outputs are IO\_Xor when s=0 from MUX 4 multiplexer and IO\_or when s=1 against MUX 4.

**Input-State Connection Table: Table 1**

DEMUX Name	Select State	Input State
DEMUX 10	0	MbW
Demux 10	1	MbA
Demux 13	0	MbA1
Demux 13	1	MbW1

**Output-State Connection Table : Table 2**

Mux Name	Select State	Output State
Mux 7	0	IO_And3
Mux 7	1	IO_or1
Mux 4	0	IO_Xor
Mux 4	1	IO_or

The two integrated circuit blocks are separated but MbA input can get the two connected into a complete circuit. This is shown in the schematic capture Figure 7:

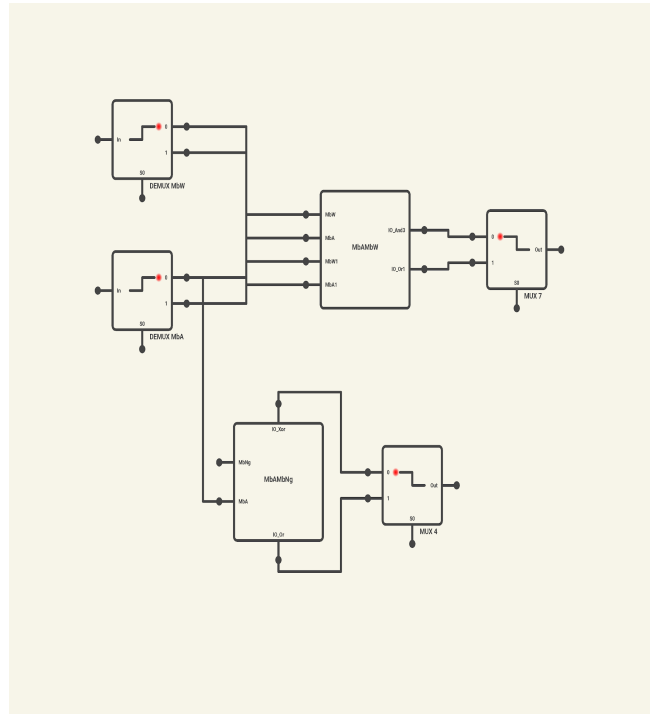


Figure 7. NB:DEMUX 10 IS DEMUX MBW AND DEMUX 13 IS NOW DEMUX MBA.

A further connection will be necessary to create a more compact integrated circuit just like a physical ic package.

This is as shown in the schematic capture :

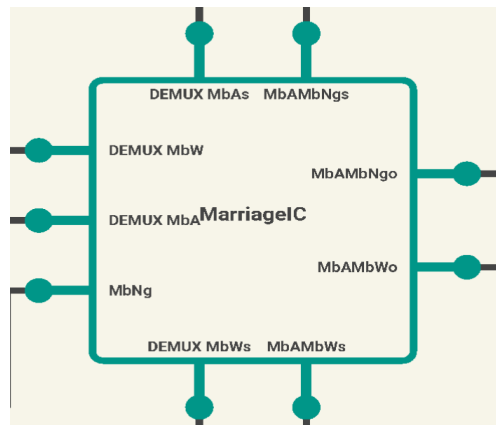
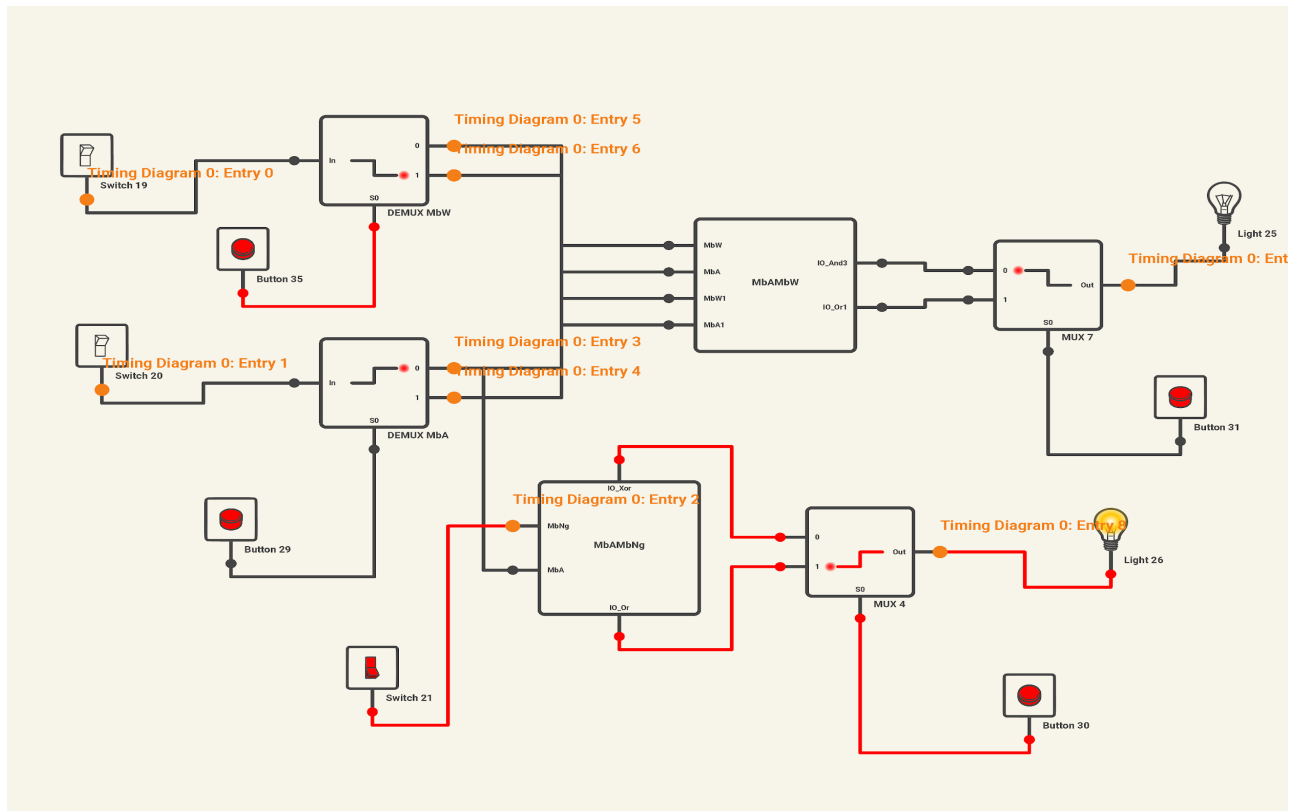


FIGURE 8.

## 2 TEST CIRCUIT DESIGN

Figure 9.



In this section, I model a circuit to test the functional design of the embedded circuits as at now. The switching test circuit as inputs with light indicators as outputs, the logic gates are put to test to assess the accuracy of functional requirements.

Henceforth, a switch component will function as a logical input to a demultiplexer that forms the switching test circuit and light /led component will function as a logical output to a multiplexer that forms the lightning test circuit.

### View on Test Circuit Design: Above Figure

Switch No.	Demux Select	Button No. / Demux	Button No./Mux	Mux select	Light /State
19	1	35/MbW	31/7	0	25/OFF
20	0	29/MbW	31/7	0	25/OFF
21	X	X	30/Mux4	1	26/ON

### Switch-Lighting State

YTT: YET TO TEST

Switch States			Indicator/Area	Demux	
19	20	21	Light	MbW	MbA
OFF	ON	ON	YTT	YTT	YTT
ON	ON	ON	ON/Top /Bot	0/1	0/1
OFF	OFF	OFF	YTT	YTT	YTT
ON	OFF	OFF	YTT	YTT	YTT
ON	ON	OFF	YTT	YTT	YTT
OFF	OFF	ON	ON/Bot	1	0
OFF	ON	OFF	YTT	YTT	YTT
OFF	ON	ON	YTT	YTT	YTT

OFF	ON	OFF	ON/Bot	0	0
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Figure 10

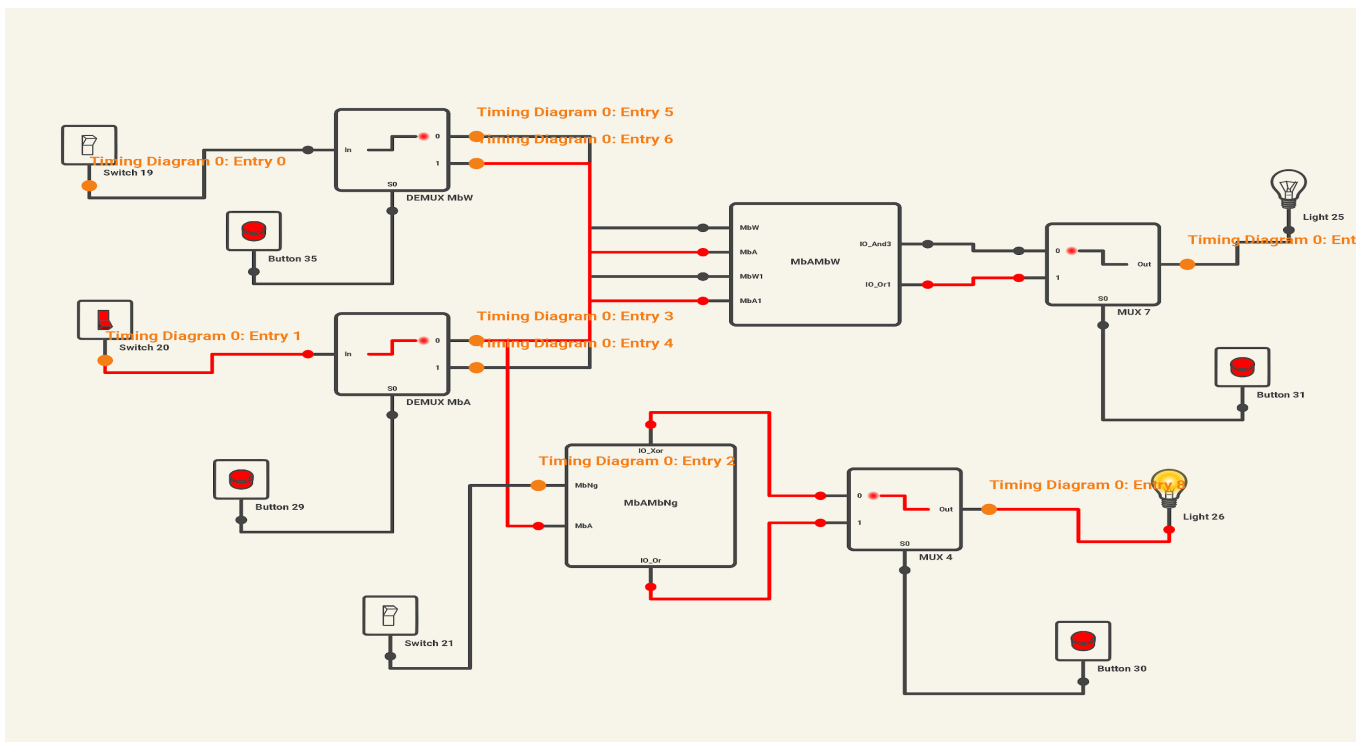
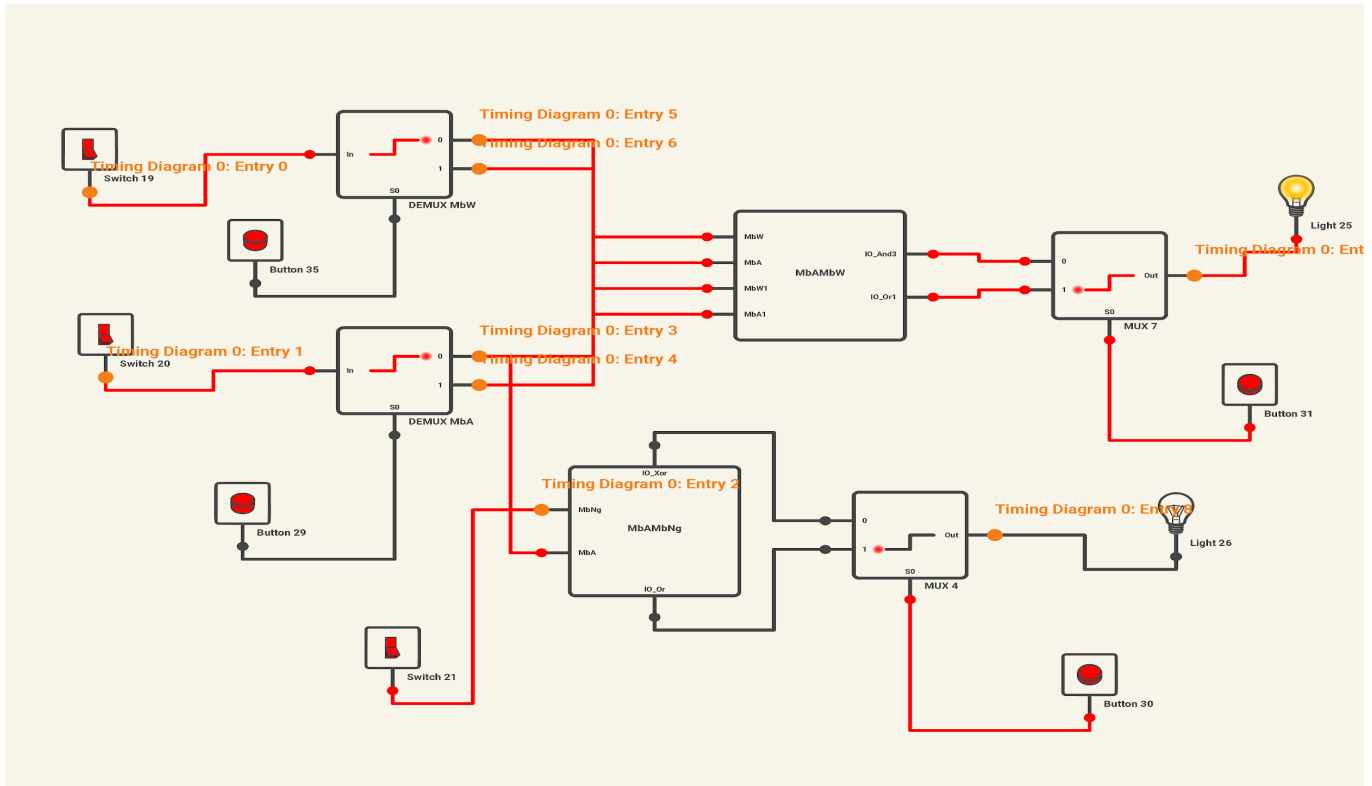


Figure 11.

### 3 FIGURES

#### 3.1 Appendices

Figure 1. Figure 8.  
 Figure 2. Figure 9.  
 Figure 3. Figure 10.  
 Figure 4. Figure 11.  
 Figure 5. Figure 12.  
 Figure 6. Figure 13.

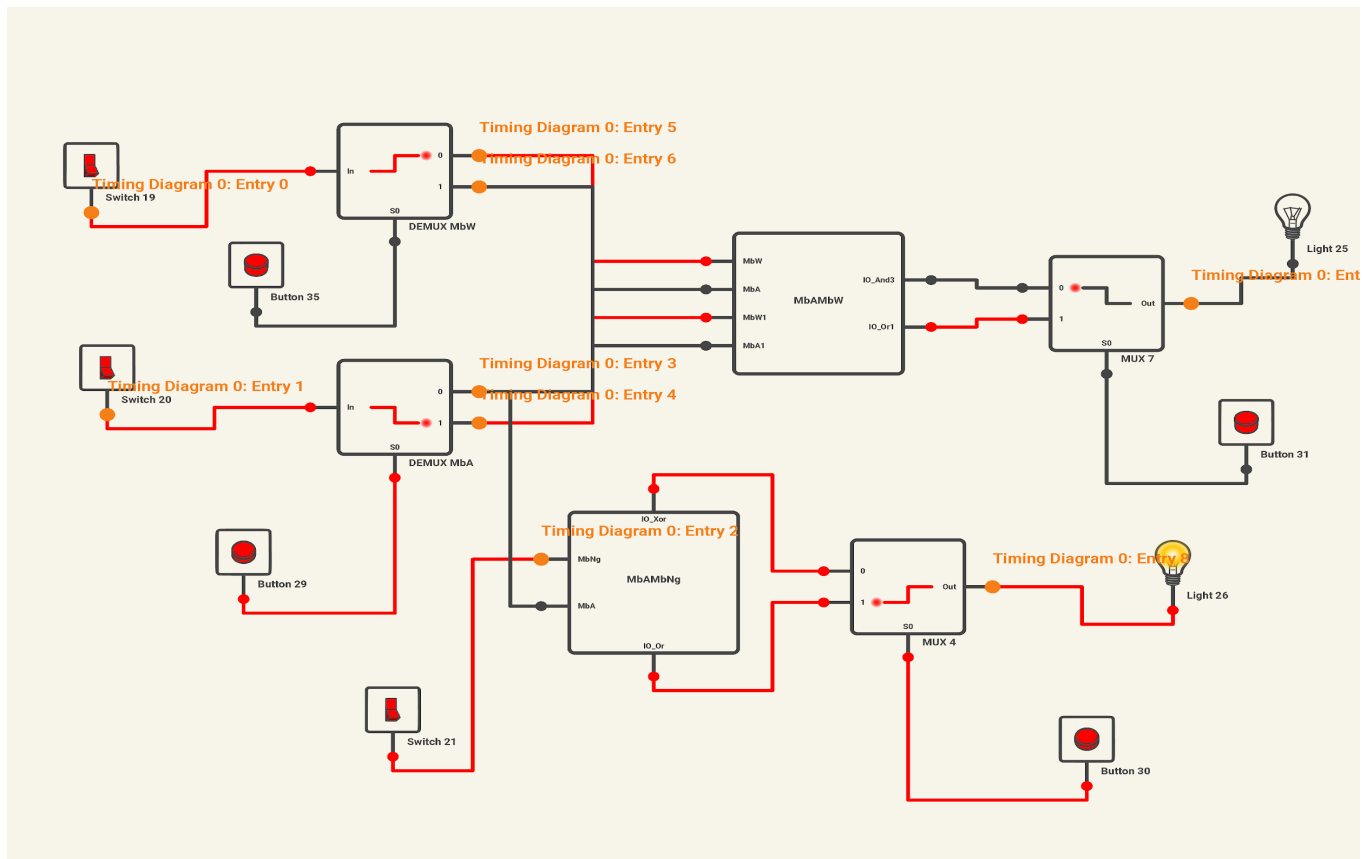


Figure 12.

### 4 CONCLUSION

This research looks mainly at essential integrated circuit design based on predicate task involving a Marriage Problem [2,3,7]. The integrated circuits are test designed with switching and (de)multiplexing circuits to make integrated lightning circuits. Finally, a view on several testing scenarios of the two ICs in generalized switch[12,13,14] and Button fashion. [15,16,17]

Figure 12.

### REFERENCES

- [1] Vingron, S. P. (2012). Logic circuit design: Selected methods. Springer Science & Business Media.
- [2] Appiah Frank. Letter Combinatorics : Theory on counting problems. EPSRC UK TuringAI Letter. 2020
- [3] Appiah Frank. Letter Combinatorics : Theory on counting problems. Marriage Problem. Mendeley Publication. 2020
- [4] Fisler, K. (1999). Timing diagrams: Formalization and algorithmic verification. Journal of Logic, Language and Information, 8(3), 323-361.
- [5] Appiah, F. (2021). Digital Logic on Marriage Problem Predicate Task (No. 5317). EasyChair.
- [6] Gates, S. C. (2004). Gate Design.

- [7] Appiah, F. (2021). A Logic Circuit Simulation on Marriage Problem Predicate with Timing Diagrams. EasyChair Preprint no. 5317, version history
- [8] Levi, I., & Fish, A. (2021). DUAL MODEL LOGIC: A New Paradigm for Digital Ic Design. Springer Nature.
- [9] Geiger, R. L., Allen, P. E., & Strader, N. R. (1990). VLSI design techniques for analog and digital circuits.
- [10] Claasen, T. A. (2003). System on a chip: Changing ic design today and in the future. IEEE micro, 23(3), 20-26.
- [11] Frank Appiah (2021). An Embedding Circuits Design on Marriage Problem Predicate in Making Integrated Circuit EasyChair Preprint no. 5317, version 5.
- [12] Chen, F., Spencer, M., Nathanael, R., Wang, C., Fariborzi, H., Gupta, A., ... & Alon, E. (2010, February). Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications. In 2010 IEEE International Solid-State Circuits Conference-(ISSCC) (pp. 150-151). IEEE.
- [13] Peng, C., Husain, I., Huang, A. Q., Lequesne, B., & Briggs, R. (2016). A fast mechanical switch for medium-voltage hybrid DC and AC circuit breakers. IEEE Transactions on Industry Applications, 52(4), 2911-2918.
- [14] Saha, S., Kumar, U. S., Baghini, M. S., Goel, M., & Rao, V. R.

(2017). A nano-electro-mechanical switch based power gating for effective stand-by power reduction in finfet technologies. IEEE Electron Device Letters, 38(5), 681-684.

[15] Krstic, S., & Theisen, P. (1986). Push-button hybrid switch. IEEE transactions on components, hybrids, and manufacturing technology, 9(1), 101-105.

[16] Kapetanakis, S., Gkasdaris, G., Angoules, A. G., & Givissis, P. (2017). Micro Switch with Wire Mini Push Button Switch. World Journal of Orthopedics, 8(12), 874.

[17] Sharp, E. D., & Hornseth, J. P. (1965). THE EFFECTS OF CONTROL LOCATION UPON PERFORMANCE TIME FOR KNOB, TOGGLE SWITCH, AND PUSH BUTTON. AEROSPACE MEDICAL RESEARCH LABS WRIGHT-PATTERSON AFB OHIO.

[18] Ehrhardt, S. M. (2020). 8mm Metal Mini Momentary 4 Pin LED Push Button Switch.

[19] Gayral, B. (2017). LEDs for lighting: Basic physics and prospects for energy savings. Comptes Rendus Physique, 18(7-8), 453-461.

[20] Grout, I. A. (2005). Integrated circuit test engineering: modern techniques. Springer Science & Business Media.

[21] Lala, P. K. (2008). An introduction to logic circuit testing. Synthesis Lectures on Digital Circuits and Systems, 3(1), 1-100.



**Dr. Frank Appiah.** He is a holder of Bsc(Hon) from Kwame Nkrumah University of Science and Technology in 2018, Msc in Advanced Software Engineering from King's college London in 2010 and PhD in computer science and engineering from both KCL (2012/2014) and KNUST (2014) respectively. Frank Appiah has professional certificates in Management and engineering since 2011 from IEEE. He developed StreamEPS - Stream Event Processing System in 2011 which is hosted at Github.

Figure 13.

